2002, by the attached Petition for Extension of Time, the attached Request for Continued Examination transmittal along with the amendments made herein by way of this Preliminary Amendment are submitted as a full and complete response thereto.

As preliminary matter, Applicant appreciates the allowance of claims 6-20. By this Preliminary Amendment, claims 1, 4 and 5 have been amended, and claim 3 has been canceled without prejudice. No new matter has been added by the amendments made herein since the subject matter recited in the claims are supported on page 8, line 30 to page 10, line 32 of the specification and shown on Figure 6 of the drawings. Accordingly, claims 1, 2, 4 and 5 with allowed claims 6-20 being pending in this application, and are respectfully submitted for a timely examination.

Claim 1 was rejected as being anticipated by Manohar et al. (U.S. Patent No. 5,963,053). Applicant respectfully traverses this rejection, and submits that claim 1 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Claim 1 recites an input circuit comprising a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other, and a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal. A first source of the first transistor and a second source of the second transistor are connected in common, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors. The input circuit further comprises a constant current source connected to the first source of the first transistor, and a current regulating circuit connected to the second source of the

second transistor and connected in parallel to the constant current source. The current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

Accordingly, the present invention provides input circuits which amplify external signals to generate internal signals having predetermined amplitudes. Furthermore, the present invention results in the advantage of having an input circuit generating internal input signals which rise and fall in response to the rising edges and the falling edges of an external input signal.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention, and therefore fails to provide the advantages which are provided by the present invention.

Manohar discloses a complementary-amplifier PECL receiver. Figure 5 of Manohar discloses a N-type amplifier 50 using n-channel differential transistors, while p-type amplifier 60 uses p-channel differential transistors. Manohar also discloses RX+ and RX- inputs which are coupled to the gates of n-channel differential transistors 56, 58 in n-type amplifier 50, and to the gates of p5 channel differential transistors 66, 68 in p-type amplifier 60. Current-mirror transistors 52, 54 are p-channel transistors in n-type amplifier 50, but current-mirror transistors 62, 64 are n-channel transistors in p-type amplifier 60. In addition, Manohar discloses node 53 which is a bias voltage set by the drain of differential transistor 56. The bias voltage of node 53 controls the current through p-channel transistors 52, 54, and the tail current n-channel tail transistor 59.

This bias voltage depends on the input voltages applied to RX+ and RX-, and the sizes of all devices including transistors 52, 56, 59.

Applicant respectfully submits that each and every element recited within claim 1 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the input circuit having current regulating transistor as recited in the present application is clearly distinct from that which is illustrated in Manohar. Specifically, it is respectfully submitted that Manohar fails to disclose or suggest an input circuit comprising a current regulating circuit connected to the differential circuit as recited in the claims.

Applicant submits that the present invention is directed to an input circuit that includes a current regulating circuit (T_{N4}) responsive to an internal signal generated at a node (drain) (N2) between a non-self-biased transistor (T_{P1}) of a current mirror circuit (6) and a data input transistor (T_{N1}) of a differential circuit (T_{N1}, T_{N2}). The current regulating circuit of the present invention is connected in parallel to the constant current source. In contrast, Manohar is merely directed to a CMOS differential receiver including a transistor (29) responsive to a voltage signal generated at a node between a self-biased transistor (22) of a current mirror circuit (22, 24) and a data input transistor (26). The node of Manohar is also connected to the gate of the self-biased transistor (22). However, Manohar does not teach or suggest the current regulating circuit of the present invention. That is, the transistor (29) of Manohar is neither comparable nor analogous to the current regulating circuit of the present invention. Furthermore, Manohar does not teach or suggest the constant current source as recited in the present application. Accordingly, it is

submitted that the input circuit of the present invention is distinguishable from that which are disclosed in Manohar.

Specifically, Manohar discloses a voltage (which does not cause the transistor (29) to cutoff) that is applied to the gate of the transistor (29) such that the consumption current of the CMOS differential receiver is maintained at constant. In other words, if a voltage of an L (low) level of CMOS is applied to the gate of the transistor in Manohar, then the transistor is turned off, so that it is not possible to maintain consumption current constant. In contrast, the constant current source of the present invention operates in response to an internal signal having an L level or a H (high) level to generate an internal signal the rising time and falling time of which are substantially the same.

Therefore, in view of the above, Applicant respectfully submits that Manohar fails to disclose or suggest each and every element recited within claim 1 of the present application.

Claims 2-5 were rejected as being unpatentable over Manohar in view of Fernandez et al. (U.S. Patent No. 5,448,200, hereinafter "Fernandez") and Harris et al. (U.S. Patent No. 5,475,323, hereinafter "Harris"). In making this rejection, the Office Action took the position that Manohar disclosed each and every element of the claimed invention with the exception of showing a delay time or a fixed current source. The Office Action cited Fernandez and Harris for curing the deficiencies which exist in Manohar.

As mentioned above, claim 3 was cancelled without prejudice, and therefore the rejection with respect to claim 3 is now moot. As for pending claims 2, 4 and 5,

Applicant respectfully traverses this rejection, and submits that each of claims 2, 4 and 5 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Fernandez discloses a differential comparator with differential threshold for local area networks or the like. Figure 1 of Fernandez discloses a differential comparator 1 with two inputs (IN+, IN-), having a master section 3 and a slave section 2. The master section 3 (having an output TSET and having inputs coupling to fixed biases $V_c+\Delta/2$, $V_c-\Delta/2$), where A is the differential threshold value for the comparator. The slave section (responsive to the two comparator inputs IN+, IN- and to the output TSET of the master section) compares signals on the two comparator inputs and produces an output (OUT+, OUT-) when the signals differentially exceed the differential threshold value. A signal on OUT+ is asserted when a signal on IN+ exceeds a signal IN- by Δ and a signal on OUT- is asserted when the signal IN- exceeds the signal IN+ by Δ.

Harris discloses an integrated circuit apparatus and method providing for utilizing voltage dividers and differential amplifiers. Harris also discloses three integrated circuit resistors R_1, R_2 and R_3. The resistors have a L_1, L_2 and L_3, and width W_1, W_2 and W_3, respectively. The voltage drop between node 101 and node 100 is Vin, the voltage drop between node 102 and node 100 is $Vout_1$, and the voltage drop between node 103 and node 100 is $Vout_2$. Harris further discloses a microelectronic resistor voltage divider 20 with linearly spaced output taps. In order to contact the voltage divider 20, accessible outputs or tap connections are provided. Adding taps to voltage divider 20 will result in the creation of parasitic tap resistance between tap connection sites 28 and 30 and main body 34 of voltage divider 20. The effect of a tap is to place parasitic resistors, r_t associated with tap in parallel with small resistor segments, r_a, of the body of the resistor

that is affected by r_t. Additionally, Harris discloses that signal distortion problems due to a common mode signal are minimized through the use of common mode feedback control circuitry 912. Common mode feedback control circuitry 912 is also connected to current sources 900 and 902 and senses the currents at nodes 914. In response to the sensed currents, common mode feedback control circuitry adjusts a variable current source 906. Variable current source 906 sinks a varying current to V_{ssa} such that the current through transistors 1000 and 1010 is maintained at constant I_D even under common mode signal conditions and independent of variations in the current source.

Applicant respectfully submits that each and every element recited within each of claims 2, 4 and 5 is neither disclosed nor suggested by the combination of prior art references. In particular, each of claims 2, 4 and 5 depends from independent claim 1, and therefore each and every limitation recited within claim 1 is also recited within each of claims 2, 4 and 5. Therefore, each of claims 2, 4 and 5 also includes the limitation of a current regulating circuit connected to the differential circuit as well as the constant current source as recited in claim 1.

As discussed above, Applicant submits that Manohar fails to disclose or suggest the limitation of a current regulating circuit connected to the differential circuit and the constant current source as recited in claim 1. Applicant further submits that this limitation is also neither disclosed nor suggested by Fernandez. Fernandez merely discloses a differential comparator that includes a master section having a differential pair 41 and a bias transistor 44 with a slave section having a differential pair 31 and a bias transistor 34. However, it is respectfully submitted that Fernandez fails to disclose or suggest a current regulating circuit and a constant current source of the present

invention. Accordingly, Applicant respectfully submits that Fernandez fails to cure the deficiencies which exist in Manohar because Fernandez fails to disclose or suggest the element of a current regulating circuit connected to the differential circuit as recited in the claims.

Additionally, Applicant submits that Harris also fails to cure the deficiencies which exist in Manohar, and/or a combination of Manohar and Fernandez. Although Harris discloses a comparator having a constant current source 904 and a variable current source 906, Applicant nevertheless submits that Harris fails to disclose a constant current source responsive to the internal signal directly. It is respectfully submitted that Harris feedback control circuit 912 merely controls the variable current source 906 such that the current through transistors 1000, 1010, is maintained at a constant. It is further submitted that the objective of Harris is to maintain a current flowing through the differential transistors 1000, 1010 at a constant by feedback control, and therefore is neither comparable nor analogous to the present invention having a uniform delay time of the rising and falling edge of internal signals relative to the external signals. Accordingly, the comparator of Harris fails to disclose or suggest a current regulating circuit as recited in the claims.

Therefore, Applicant respectfully submits that neither Manohar, nor Fernandez, nor Harris, taken alone or in combination, disclose or suggest each and every element recited within claims 2, 4 and 5 of the present application.

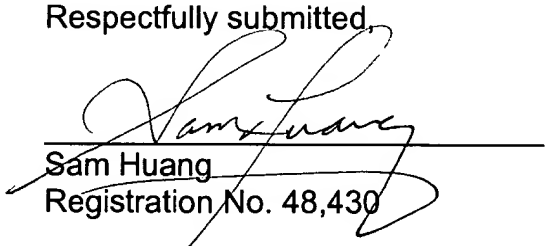
In view of the above, Applicant respectfully submits that claims 1, 2, 4 and 5, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that this subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 1, 2, 4 and 5 be found allowable, and that this application be passed to issue along with allowed claims 6-20.

If for any reason the Examiner determines that this application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,



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Petition for Extension of Time (1 month)

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MARKED-UP COPY OF ORIGINAL CLAIMS 1, 4 and 5

1. (Three Times Amended) An input circuit comprising:

a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other;

a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal, wherein [sources of the first and second transistors] a first source of the first transistor and a second source of the second transistor are connected in common, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors;

a constant current source connected to the first source of the first transistor; and

a current regulating circuit connected to [the differential circuit] the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

4. (Amended) The input circuit according to claim [3] 1, wherein the constant current source is connected to a high potential power supply, and wherein the current regulating circuit includes a third transistor connected in parallel to the constant current source, the third transistor going ON and OFF in response to the internal signal.

5. (Amended) The input circuit according to claim [3] 1, wherein the constant current source is connected to a low potential power supply, and wherein the current regulating circuit includes a third transistor connected in parallel to the constant current source, the third transistor going ON and OFF in response to the internal signal.